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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

Inventor(s): Craig Nemecek

Group Art Unit: 2825

Filed: 11/15/01

Examiner: THOMPSON, A. M.

Serial No.: 09/998,859

Title: A SYSTEM AND A METHOD FOR CHECKING LOCK STEP CONSISTENCY BETWEEN AN IN
CIRCUIT EMULATION AND A MICROCONTROLLER WHILE DEBUGGING PROCESS IS IN
PROGRESS

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub- class	Filing Date
	A						
	B						
	C						
	D						
	E						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub- class	Translation	
							Yes	No
	F							
	G							
	H							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
		"PSoC Designer: Integrated Development Environment" User Guide; Revision 1.11; CMS10005A; Last Revised: 7/17/01; Cypress MicroSystems, Inc.
Examiner		Date Considered 27 October 2004

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.